

**SEMICONDUCTOR MEMORY DEVICE TESTABLE WITH A SINGLE  
DATA RATE AND/OR DUAL DATA RATE PATTERN IN A MERGED  
DATA INPUT/OUTPUT PIN TEST MODE**

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Abstract of the Disclosure

Provided is a semiconductor memory device testable with a single data rate (SDR) or a dual data rate (DDR) pattern in a merged data input/output pin (DQ) test mode. The device includes a first path circuit, a second path circuit, and a merged output generator configured to generate a 10 merged data bit having a SDR and/or DDR pattern.